AN7610
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- 1 GSPS Conversion Rate
- On-Board Reconstruction DAC
- On-Board Reference Circuit
- On-Board Adjustable Reference
- Decimated Digital Data Output
- Selectable Decimation Divide by 16/32/64 Options

APPLICATIONS

- Evaluation of SPT7610 6-Bit ADCs
- Engineering System Prototype Aid
- Guide for Design of SPT7610 Interface Circuitry
- Guide for Design of SPT7610 PCB Layout

SPECIAL REQUIREMENTS

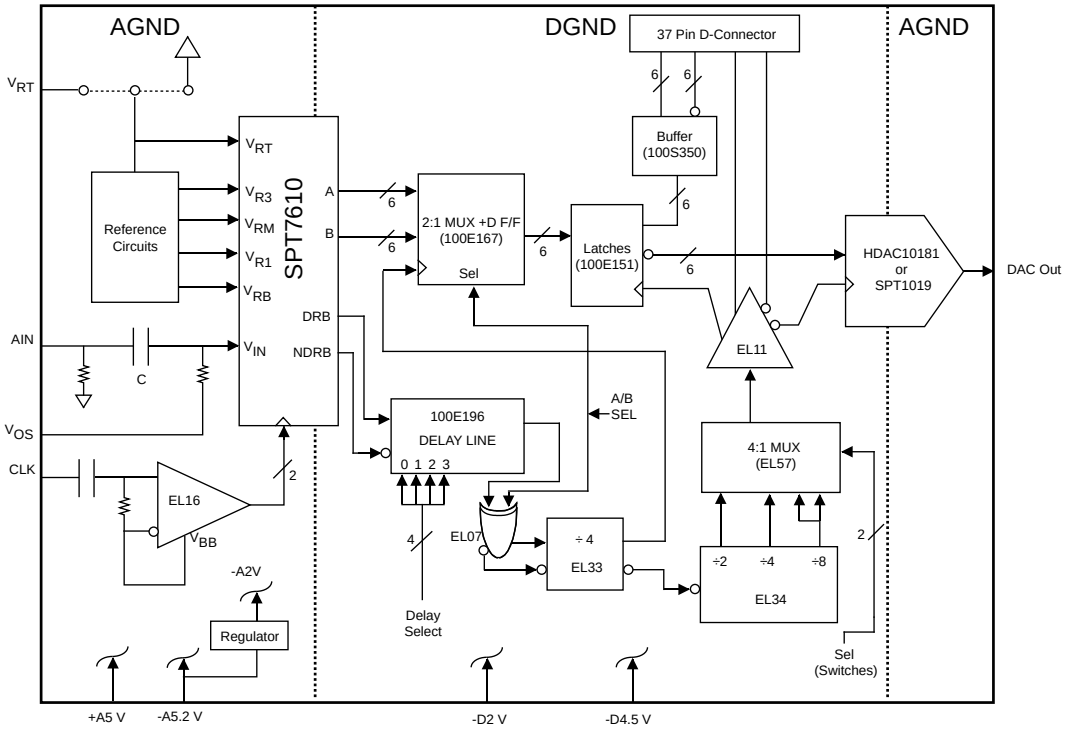
The SPT7610 device requires adequate heat sinking and air flow for optimum performance.

GENERAL DESCRIPTION

The EB7610 evaluation board is specifically designed for device characterization and demonstration of the performance of the SPT7610 A/D converter. The SPT7610 has a guaranteed sample rate of 1 GSPS. At this high conversion speed, hand-crafted bread boards will not perform effectively, and a printed circuit board is a must. This application note should be used as a supplement to the SPT7610 data sheet to aid designers in achieving optimal device performance.

The EB7610 comes with the SPT7610SIQ in an 44-lead cerquad surface mount package directly soldered to the board for optimum performance. The EB7610 is capable of operating at clock rates up to 1 GSPS. (Clock rates higher than 1 GSPS are possible but not guaranteed.) The block diagram of the board is shown in figure 1. Note that adequate air flow and a heat sink are necessary for optimum performance of the ADC.

Figure 1 - Block Diagram, Rev C



Signal Processing Technologies, Inc.

4755 Forge Road, Colorado Springs, Colorado 80907, USA

Phone: (719) 528-2300 FAX: (719) 528-2370

SPT7610 ADC OVERVIEW

The SPT7610 has a guaranteed minimum sample rate of 1 GSPS. Only one -5.2 V power supply is required. Two external references are applied across the internal reference ladder that has a resistance of 80 Ω typical (60 Ω minimum). The top reference is typically 0 V or connected to AGND (analog ground). The device has top force and sense pins (V_{RFT} and V_{RST}) that are internally connected together. These voltage force and sense pins can be used to minimize the voltage drop across the parasitic line resistance.

The bottom reference is typically -1 V. The device also has bottom force and sense pins (V_{RFB} and V_{RSB}) that are internally connected together. These can also be used to minimize the voltage drop across the parasitic line resistance. Three additional reference taps (V_{R3} = -0.25 V typ, V_{RM} = -0.5 V typ, and V_{R1} = -0.75 V typ) are brought out. These taps can be used to control the linearity error.

All logic levels are compatible with both 10K ECL or 100K ECL. It is recommended that the clock input be driven differentially (CLK and NCLK) to improve noise immunity and reduce aperture jitter.

The digital outputs are split into two banks of 6 bit words and an overrange bit. Each bank is updated at 1/2 of the input clock rate and are 180° out of phase from each other. The differential data ready signals for each bank are provided to accurately latch each data bank into the register. The output data is in a straight binary, inverted binary, two's complement or inverted two's complement format. (Refer to the data sheet for details.) Figure 2 shows a timing diagram of the device and shows the input to output relationship, clock-to-output delay and output latency. The SPT7610 has a built-in offset in the ÷2 clock divider (D Flip-Flop) to assure that output bank A will come up first after power turn on.

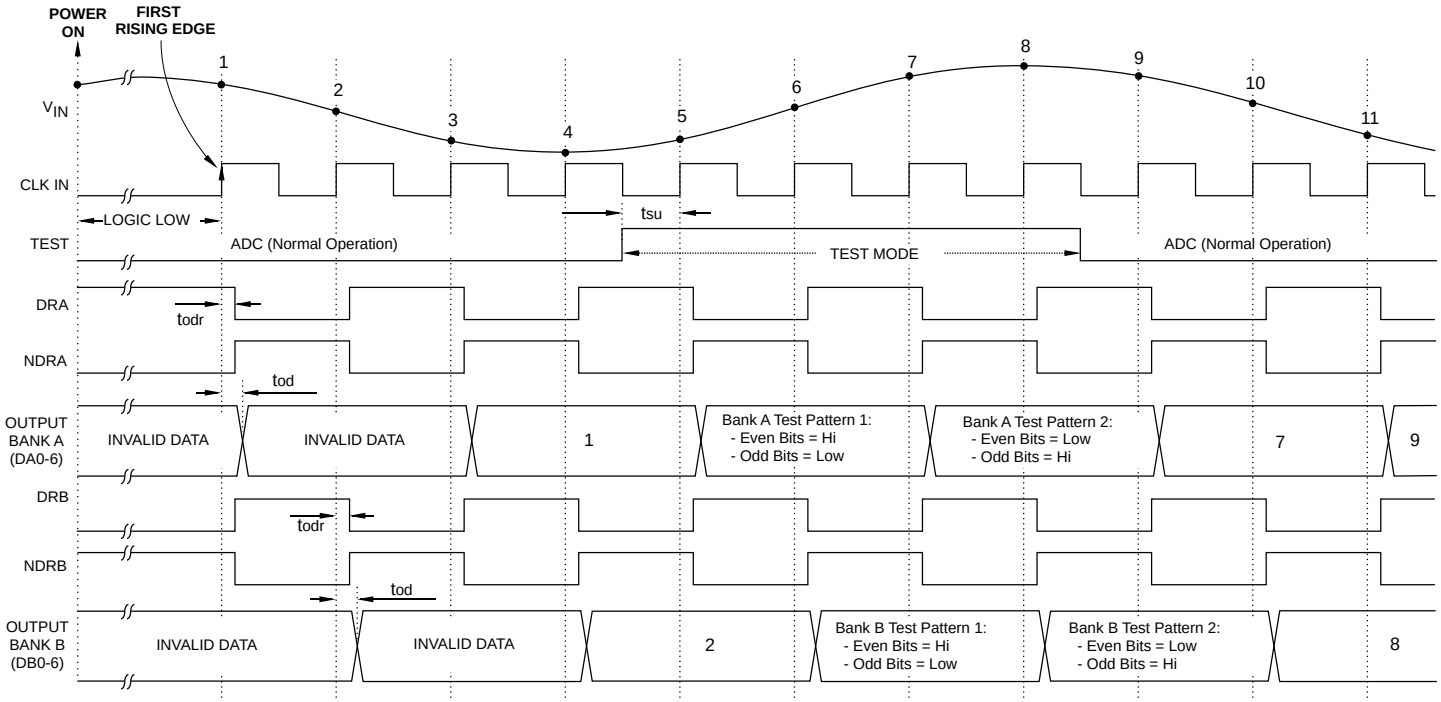
The full scale analog input bandwidth is 750 MHz (1.4 GHz for small signal bandwidth). The input capacitance is 8 pF (typical). Power dissipation is specified at 2.85 W maximum at +25 °C. **Adequate air flow and a heat sink are necessary.** The data sheet provides the required information necessary for heat sink selection and indicates the required air flow rates. Refer to the Thermal Management section of the SPT7610 data sheet.

SPT7610 TEST MODE FUNCTION

The SPT7610 supports a special test mode function that overrides the SPT7610's internal data output latch stage and excercises the digital outputs in an alternating test pattern. This enables the user to test digital interface logic downstream from the SPT7610 with a known set of digital test patterns.

Test mode pin 3 controls the SPT7610 mode of operation such that when it is low, the SPT7610 operates in normal mode. When test mode pin 3 is brought high, the SPT7610 will begin to output test pattern 1 (see table I) on the next rising edge of the clock. (See figure 2.) It will output the test patterns alternating between test pattern 1 and test pattern 2, as long as test mode pin 3 is held high. The minimum set-up time (tsu) can be as low as 0 nsec.

Figure 2 - SPT7610 Timing Diagram



Only the digital output stage is involved in the test mode operation. All ADC stages before the digital output stage continue normal data conversion operation while test mode is active. When test mode pin 3 is brought back low, the SPT7610 will resume output of valid data on the next rising edge of the clock. The valid data output will correspond to a two clock cycle pipeline delay as shown in figure 2.

Table I - SPT7610 Test Mode Output Bit Patterns

	D6	D5	D4	D3	D2	D1	D0
Test Pattern 1	1	0	1	0	1	0	1
Test Pattern 2	0	1	0	1	0	1	0

OPERATION AND CALIBRATION

POWER SUPPLIES AND GROUNDING

Inside the SPT7610 every circuit is biased from AGND to V_{EE} (analog), except the DGND pins. This includes the clock input circuitry. To minimize any ground loops and to optimize performance, all interfacing circuits must be referenced to the appropriate grounds.

The reference, analog input and clock input drivers are to be referenced to AGND. The DGND pins, digital output loads and all logic interfacing circuits are to be referenced to DGND. The block diagram on page 1 indicates clearly where the AGND and DGND are split. The AGND and DGND are tied to each other through a ferrite bead as closely to the converter as possible. The EB7610 requires three power supplies as listed in the table below.

Table II - EB7610 Power Supply Requirements

Supply	Voltage Range (V)			Typical Current
	Min	Typ	Max	(mA)
-A5.2 V	-4.95	-5.2	-5.45	1000
-D2 V	-1.95	-2.0	-2.2	1200
-D4.5 V	-4.20	-4.5	-4.8	500

Figure 3 is the recommended power supply hookup for the evaluation board. SPT recommends that all power supplies be turned on and off at the same time via a power strip.

Figure 3 - Configuration of Power Supplies

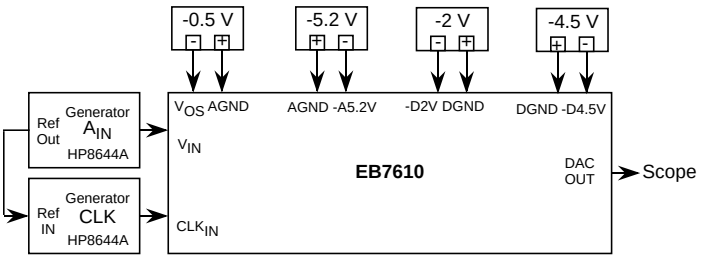


Table III - Initial Set Up of Board Jumpers/Dip Switches

Option Jumpers	Status	Switch	Status
J1B	Short	J6A, J1A	Open
J2	Short	J6B	Open
J3	Short	J9A	Short
J4	Short	A/B SEL	LO or HI
J5A	Short	S0	HI
J5B	Short	S1	HI
		S2, S3, S4, S5, S6	LO

PROCEDURE FOR VERIFYING BOARD OPERATION

To verify correct board operation:

- Connect power supplies and generators (leave off).
- Set jumpers and dip switches to proper configurations. (See table III.)
- Turn on clock generator and set to 499.712 MHz and 1 Vp-p.
- Turn on analog input generator and set to 3.965 MHz and 1 Vp-p.
- Turn all power supplies on and observe the 61 kHz sinewave at the scope (64 points/period).

Refer to Beat Frequency Technique section for more detail.

REFERENCE CIRCUIT

Referring to figure 8, D1 is a 1.2 V Zener diode. R8 and R1 potentiometers are used as a reference adjustable voltage to give -1.0 V ±0.005 V at the V_{REF} test point. This voltage is then buffered with U4A and drives Q1 that is set up as an emitter follower. The emitter follower is necessary to sink up to 17 mA through the reference ladder (based on 1 V reference and 60 Ω minimum ladder resistance). U4 (a low voltage rail-to-rail quad op-amp) is powered from GND to -5.2 V. The selection of U4 prevents the reference from going positive during power on and keeps it to within the maximum rating (+0.5 V to V_{EE}).

The top reference is connected to AGND if J1B is installed. The top reference may be driven externally through the V_{RT} banana jack (with respect to AG3 banana jack) by installing a jumper at J1A instead of a jumper at J1B.

The SPT7610 has three reference ladder taps brought out. These taps can be forced to their theoretical voltage to correct the bow in the transfer curve due to the injection of the pre-amp input bias currents into the reference ladder. V_{R3} is the 1/4 scale tap, V_{RM} is the mid-scale tap, and V_{R1} is the 3/4 scale tap. For example, when V_{RTF} = 0 V and V_{RBF} = -1.0 V, V_{R3}, V_{RM} and V_{R1} should be forced to -0.250 V, -0.500 V and -0.750 V respectively. Each tap is provided with its test point. The potentiometers R2, R3 and R4 are provided for voltage adjustments to the taps.

A 2.2 µF decoupling capacitor in parallel with 0.1 µF and 100 pF surface-mount capacitors is recommended for all reference pins (V_{RTF}, V_{R1}, V_{RM}, V_{R3} and V_{RBF}). These capacitors should be placed as close to the pin as possible. (The smallest value should be the closest.)

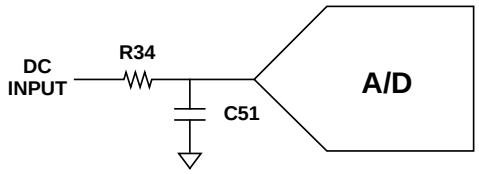
ANALOG INPUT

SPT was not able to locate an op-amp suitable to drive the SPT7610. It requires a bandwidth of at least 800 MHz and at least -40 dB of distortion. Given an input capacitance of 8 pF, the required peak driving current is $2\pi fC$ = 20 mA, for f = 400 MHz.

For AC input into the EB7610, connect the analog input into the V_{IN} SMA. C51 is for coupling to the DUT. Applying -0.5 V to the V_{OS} banana jack (referenced to AGND) will offset the input to meet the 0 to -1 V input range of the A/D.

If DC input is required, inject the analog input through the V_{OS} test point and place a ground cap on the V_{IN} BNC. Figure 4 shows the DC coupled input circuit with this configuration. Note: R34 is socketed.

Figure 4 - DC Coupled Input Configuration



CLOCK CIRCUIT

The clock input driver uses a MC10EL16 (U3) which is a single, 10K, ECL family logic differential line receiver. Its input is set up for AC coupling from a 1 Vp-p (CLK IN) with R35 (49.9 Ω terminating resistor) connected to V_{BB}. **The CLK IN signal (1 Vp-p ±10%) must be present to prevent U3 from oscillating as the two inputs are balanced. It is important to note that the input common mode range for U3 is -0.4 V maximum.** U2 is a -2 V regulator (from analog -5.2 V) used only for U3 output load pull down. Note that the clock circuits are biased from the analog supply. This is critical to maintain the optimum performance.

CLK and NCLK test points are provided on board. These test points physically resemble those in the schematic. The physical layout of the test points provides a short ground path to the scope probe ground.

EB7610 CALIBRATION

All measurements are with respect to AGND.

- Hook up power supplies as shown in figure 3.
- Refer to the initial setup section for jumper/switch setup.
- Turn all power supplies on.
- Monitor the -A2 test point with DVM and adjust the R5 potentiometer for -2 V ±10 mV.
- Monitor the SB test point with DVM and adjust the R4 potentiometer for -1 V ±5 mV.
- Measure/record V_{FT} and V_{FB} test points with DVM.
- Monitor the V_{R3} test point with DVM and adjust the R2 potentiometer for $\frac{V_{FB} - V_{FT}}{4} + V_{FT}$.
- Monitor the V_{RM} test point with DVM and adjust the R3 potentiometer for $\frac{V_{FB} - V_{FT}}{2} + V_{FT}$.
- Monitor the V_{R1} test point with DVM and adjust the R4 potentiometer for $\frac{3(V_{FB} - V_{FT})}{4} + V_{FT}$.

DIGITAL OUTPUT BUFFER/DECIMATION CIRCUIT

With the exception of U3 (10K logic family), all interfacing logic chips (U8-U16) are 100K logic family. The SPT7610 requires an immediate digital output buffer. The digital outputs are compatible with both 10K or 100K ECL logic families. All digital outputs are pulled down to digital -2 V through 49.9 Ω resistors. U8 is the Motorola MC100E167, 2:1 MUX register. Each 6-bit digital output bank A or bank B is selected through U8 with an A/B switch. The selected data bank is updated at the rate of the data ready signal divided by 4:

- U11 is a programmable delay.
- U12 is the exclusive-or acting as a buffer or inverter with the A/B switch (S2).
- U13 is the divide-by-4 counter.

Note that the data ready signals for bank A and for bank B are opposite in phase. (See the SPT7610 timing diagram.)

U8 requires a minimum of 100 ps of setup time and 300 ps of hold time. To meet these requirements, set delay switches S0-S3 to logic Ø (down) and set R7 to mid-range. R7 is a fine tune delay control for U11, which gives a range of 0 to 80 ps from 0 to -4 V.

The second decimation is through U9 which is a hex D flip flop. U14 is the ÷2, ÷4, ÷8 clock generation chip. The desired divider value is selected through U15 (4:1 MUX) with SØ and S1 switches. (See table V.)

U16 is a clock distributor for U9, U5 (DAC) and the P1 connector.

Table IV - SØ, S1 Set Up

S1	SØ	Overall Decimation (N) With Respect to f_{CLK}
0	0	64
0	1	64
1	0	32
1	1	16

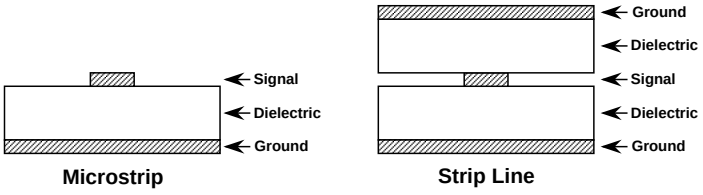
DATA RECONSTRUCTION DAC

The decimated encoded data is reconstructed and the signal can be viewed through the DAC OUT SMA. U24 (SPT1018 or SPT1019) is a 275 MWPS, 8-bit video DAC. It is set up for a fixed gain with an output range from 0 to -19 mA into a 51 Ω Load (R90 socket) or 0 to -960 mV. A larger output voltage range can be attained by replacing R90 with a larger value as long as the output stays within the DAC output compliance voltage range of -1.2 V.

BOARD LAYOUT AND DESIGN CONSIDERATIONS

Both Microstrip and Strip Line PCB board technologies have predictable characteristic impedances that can be controlled to within 5%. Figure 5 shows the basic cross section of each technology. For G-10 dielectric material, the propagation delay of the line is typically 148 ps/in for Microstrip and 188 ps/in for Strip Line. Note that the propagation delay is independent of line width.

Figure 5 - Cross Sections of Microstrip and Strip Line PCB Board Technologies



Due to the complexity of the EB7610 design, both techniques were used to make routing easier. The line width is 10 mil and has a 50 Ω characteristic impedance. It is an eight layer board stacked in the following manner:

Layer 1=First controlled impedance signal layer (Microstrip)
Layer 2=Ground layer *
Layer 3=Second controlled impedance signal layer (Strip line)
Layer 4=Ground layer *
Layer 5=Third controlled impedance signal layer (Strip line)
Layer 6=Ground layer *
Layer 7=Power layer - all supplies share the same layer
Layer 8=Fourth controlled impedance signal layer (Microstrip)
* AGND & DGND share the same layer.

To minimize the logic skew, the line lengths in each stage are closely matched to within 0.05 inch, especially between the A/D output and the second decimation circuit (U8).

The following is an outline of some of the key guidelines used in the design of the EB7610 evaluation board:

1) Minimize the logic fan-out. Most of them have a fan-out of only one.
2) Avoid, if possible, any through-hole vias between the sending and receiving end of any high speed lines. A pin-out pattern of the logic that requires criss-crossing of high speed lines should be avoided if possible.
3) The loading resistor should be as close to the receiving end as possible on all high speed lines.
4) All unterminated (open) lines must be less than 1/4 of the rise time of the signal divided by the transmission line propagation delay to assure minimal reflection:

   Open Line Length (inches) < 1/4 x (trise / tpd)

   where: trise = rise time of the signal (ns)
   tpd = 0.188 ns/in (Strip Line characteristic)
   tpd = 0.148 ns/in (Microstrip)

   Table V shows the typical rise times versus the major high speed logic families with a fan-out of one.
5) Use a series damping resistor when an open line exceeds the 1/4 x (trise / tpd) maximum.
6) Keep the analog circuitry separate from the digital circuitry including isolation of grounds. AGND and DGND must be tied together through a ferrite bead or an inductor as close to the A/D as possible.
7) Ensure adequate decoupling of the supplies.
8) Surface mount resistors and capacitors work better for high speed designs.

Table V - Typical Rise Times versus Major High Speed Logic Families

	ECL 10K	ECL 10KH	SYNERGY 100E	SYNERGY 100S	SPECL SONY
$t_{rise\ (ns)}$	2-3.5	1.1	0.3-0.4	0.7	0.3-0.4

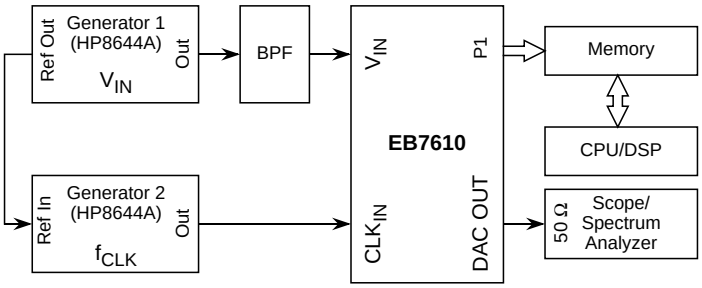
CHARACTERIZATION OF THE SPT7610 USING THE EB7610 EVALUATION BOARD

This section has recommendations for how to best characterize the SPT7610 using the EB7610 evaluation board. The intent is to provide some basic principles and methods of characterization that will enable the optimal performance of the SPT7610 to be viewed and characterized so the proper design considerations can be made.

RECOMMENDED TEST SET UP

Figure 6 shows a simple block diagram of the recommended test set up.

Figure 6 - AC Test Set-Up Block Diagram



SELECTION OF GENERATORS

At higher analog input frequencies selecting the signal sources becomes very critical in order to minimize system induced measurement error. Two considerations for generator selection are jitter and purity.

Generator Jitter Requirements

One of the key parameters in the selection of the signal sources is the phase jitter or aperture uncertainty. Jitter is caused by instability in the time base of the generated signal. This will appear as an erroneous voltage error at the sampled point. The source jitter must be kept below an allowable level so that accurate characterization of the conversion device can be conducted. The induced voltage error due to jitter is directly proportional to the analog input slew rate (Sr). The highest slew rate is at mid-scale.

$Sr = \Delta V / \Delta t = \pi f$ Slew rate for a 1 Vp-p sinewave
$Tj = \Delta t = \Delta V / \pi f$ Time jitter or aperture jitter

For example, if a 1 Vp-p analog input sinewave is used as the source and if 0.2 LSB of error caused by the signal source is acceptable, then the aperture jitter calculates as follows:

$Tj = \Delta V / \pi f$
allowable $\Delta V = (1 \times 0.2) / 64 = 3.125$ mV
For f_{IN}= 400 MHz the allowable source jitter is Tj = 2.5 ps

SPT recommends using the Hewlett Packard, HP8644A frequency generator that is specified to have 0.7 ps RMS of phase jitter.

Source Purity

Another parameter that needs attention is the purity of the signal source used for the analog input. A suitable band pass filter (BPF) may be needed between the signal source and the EB7610 input (V_{IN}).

Alternately, a notch filter can be inserted to suppress the highest harmonic in the signal source. A simple notch filter can be constructed from a coaxial cable (or twisted wire) stub cut to a quarter wave length. See figure 7. The velocity or speed of the signal depends on the conductor material used in the stub. Table VI shows signal propagation rates for several conductor types.

Figure 7 - Stub Interconnection

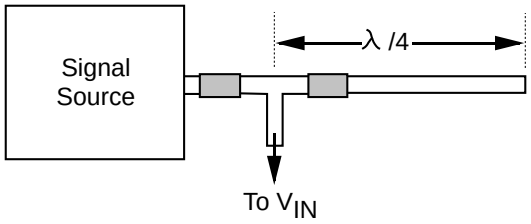


Table VI - Signal Propagation Rates by Conductor Type

Conductor	Speed (v)
Any conductor in air	30 cm/ns
Microstrip Line (epoxy)	15 cm/ns
Coaxial Cable (Teflon)	20 cm/ns

The wave length $\lambda = v / f$ where f = frequency of interest. Use a network analyzer or simply use an oscilloscope to precisely cut the stub to $\lambda/4$.

CHARACTERIZATION USING DECIMATED DATA OUTPUT

The SPT7610 is sampled at 1 GSPS with an output data rate of half the clock rate (500 MHz). Given this very high data rate, there is no simple tool to analyze the data without development of a tedious breadboard involving demultiplexers, high-speed memory fan out, etc.

The EB7610 provides the user with decimated data output (by factors of 16/32/64 with respect to the input clock) at the P1 connector and the DAC output.

Beat Frequency Technique

The beat frequency technique is highly recommended when characterizing the SPT7610 using the decimated data output from the P1 connector or DAC output BNC. Three parameters must be properly selected for the beat frequency technique to work:

fs = Sampling frequency or CLK IN to EB7610
f_{IN} = Analog input frequency
N = 16/32/64, decimation factor (See table V)

The input frequency is calculated as follows:

$f_{IN} = n\ Fc \pm Fb$
where:
fc = fs/N Capture frequency (Decimated frequency at P1)
n = integer
fb = fc / S Beat frequency
S = Number of sample points

EXAMPLE
Capturing a 4096 point FFT at the P1 connector with the following constraints is desired:
fs = 750 MHz
fin = 50 MHz and 100 MHz
Maximum update rate of the memory = 20 MHz

Solution:

a. For N = 64

$$fc = fs / N = \frac{750 \times 10^6}{64} = 11.71875 \text{ MHz} < 20 \text{ MHz}$$

b. The beat frequency:
fb = fc/4096 = 2861.022949 Hz

c. Round off fb to eliminate round off errors and to improve source resolution:
fb = 2860, then work backwards:
fc = fb x 4096 = 11.71456 MHz
fs = fc x 64 = 749.73184 MHz

d. For n = 4, fin = 4 x fc + fb = 46.8611 MHz
For n = 9, fin = 9 x fc - fb = 105.4339 MHz

e. Conclusions
fs = 749.73184 MHz
f_{IN} = 46.861101 MHz and 105.4339 MHz
N = 64

For convenience, table VII shows example setup parameters for 4096 point beat frequency tests.

Table VII - 4096 Point Beat Frequency Test Set Up

fs (MHz)	f_{IN} (MHz)	N (Decimation)	fc (MHz)	fb (Hz)	n
500.039680	46.882535	32	15.62624	3815	3
500.039680	109.387495	32	15.62624	3815	7
500.039680	156.266215	32	15.62624	3815	10
500.039680	203.144935	32	15.62624	3815	13
500.039680	296.902375	32	15.62624	3815	19
500.039680	406.286055	32	15.62624	3815	26
749.731840	46.861100	64	11.71456	2860	4
749.731840	105.4339	64	11.71456	2860	9
749.731840	152.29214	64	11.71456	2860	13
749.731840	199.15038	64	11.71456	2860	17
749.731840	304.58142	64	11.71456	2860	26
749.731840	398.2979	64	11.71456	2860	34
1001.39008	46.94398	64	15.64672	3820	3
1001.39008	93.88414	64	15.64672	3820	6
1001.39008	156.47102	64	15.64672	3820	10
1001.39008	203.41118	64	15.64672	3820	13
1001.39008	297.2915	64	15.64672	3820	19
1001.39008	406.81854	64	15.64672	3820	26

Method 1 - Characterization Through the DAC Output

With the set up in table VII, the DAC output signal would be a sinewave at fb and consists of 4096 points/period (1/fb). The DAC reconstruction signal is used to ensure proper setup of the evaluation board and can be used directly for characterization purposes. The performance of the device can be viewed from DAC Out signal with a spectrum analyzer.

The analog input offset and gain can be adjusted by monitoring the DAC Out with a scope.

The DAC Out signal can be used to verify the delay of the clock to the first stage decimation so that the setup and hold times are met. Refer to the Digital Output Buffer/Decimation Circuit section and set the delay line switches accordingly until no glitches or spikes appear in the DAC output signal.

Method 2 - Noise Characterization Through DAC Output

Noise is inherent to an ADC as a DC noise or noise floor. It could be identified simply by inputting a DC input and measuring the number of code counts. The simplest and more accurate way to measure this noise is to input a slow ramp and measure the code transition noise through the DAC output. The slope of the ramp input suggests at least 10 capture data per LSB or slope $\leq$(LSB x f_C)/10.

With certain types of ADCs, this transition code noise changes with the input frequency. The beat frequency technique offers a tool for characterizing the code transition noise at higher input frequencies. Table VII is the set up for S = 4096 points per beat period. The code transition noise could be viewed through DAC out with a scope by reducing S to a much smaller number of points per period (32 or 64 points).

Method 3 - Characterization Through the P1 Connector

From table VII, 4096 points FFT can be performed from the data output at P1 (37 pin D shell connector). Refer to the detailed schematic in figure 8 for the pin assignment. Note that the reconstruction DAC output signal should be used before an FFT is taken to verify proper setup of the evaluation board (decimation setup and delay line switches) and analog input signal (offset and gain).

Figure 8 - Detailed Schematic, Rev C

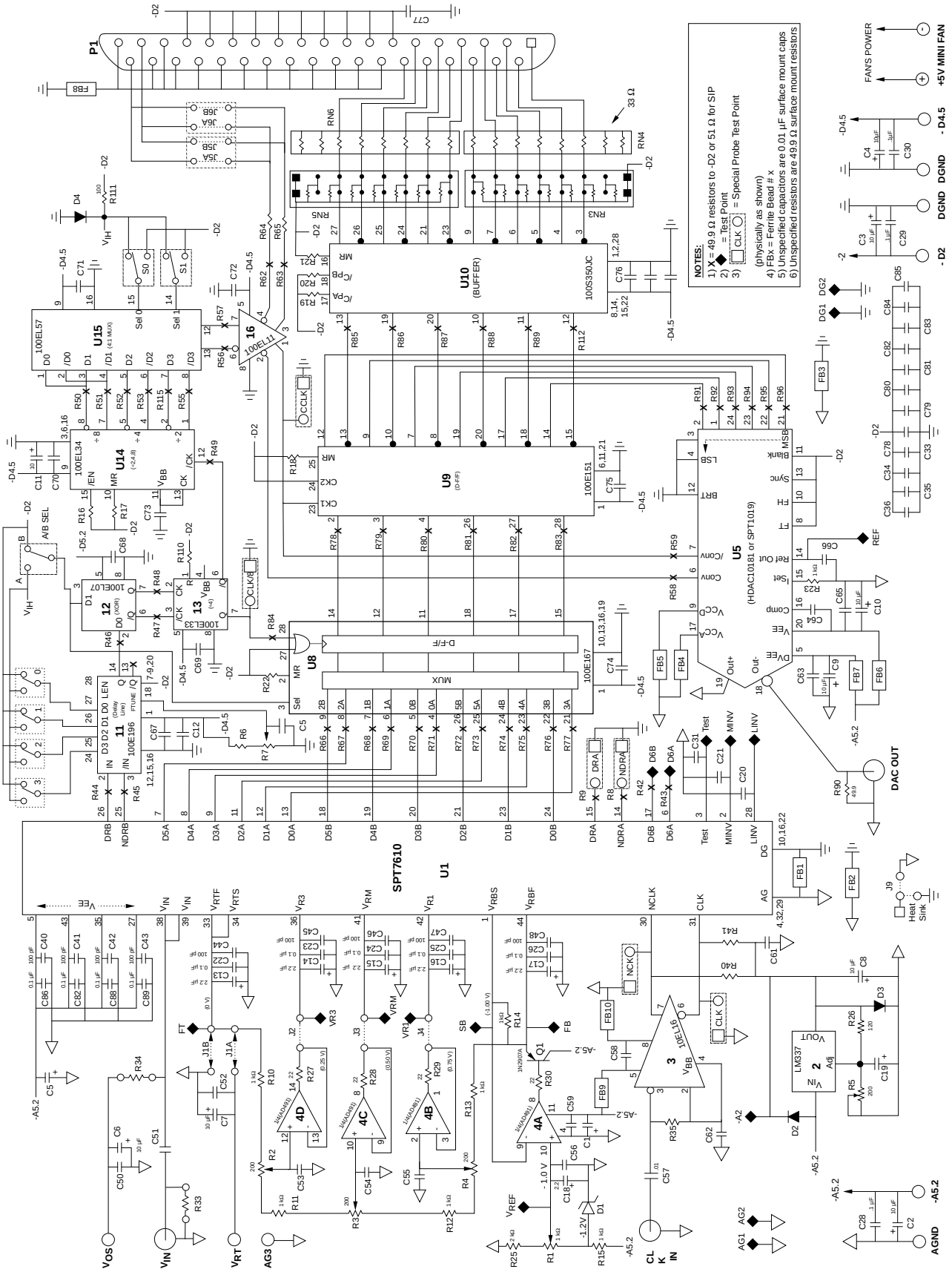
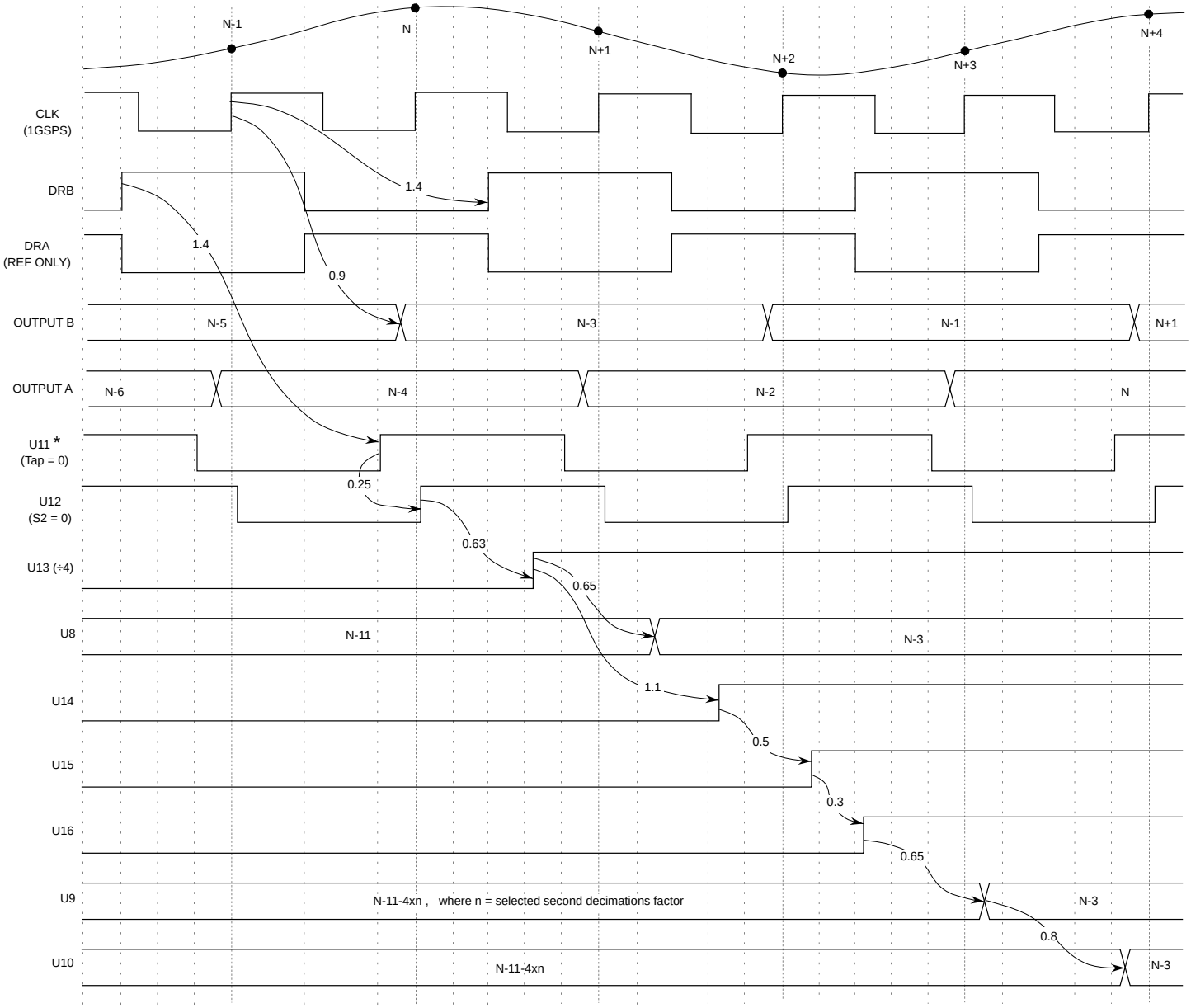


Figure 9 - Timing Diagram, Rev C



***U11 output has a delay of 1.4 ns. See table VIII for addtional delay times.**

Table VIII - U11 Output Delay Table

S6	S5	S4	S3	Typical Additional Delay (ps)*	Typical Total Delay (ps)*	S6	S5	S4	S3	Typical Additional Delay (ps)*	Typical Total Delay (ps)*
0	0	0	0	0	1,400	1	0	0	0	140	1,540
0	0	0	1	18	1,418	1	0	0	1	158	1,558
0	0	1	0	35	1,435	1	0	1	0	175	1,575
0	0	1	1	53	1,453	1	0	1	1	193	1,593
0	1	0	0	70	1,470	1	1	0	0	210	1,610
0	1	0	1	88	1,488	1	1	0	1	228	1,628
0	1	1	0	105	1,505	1	1	1	0	245	1,645
0	1	1	1	123	1,523	1	1	1	1	263	1,663

*FTune has a range from 0 to 80 ps, 0 to -4.0 V respectively.

EB7610 BILL OF MATERIALS

#	Ref Des	Description	Vendor	Part Number	Qty
1	(2) AGND, V_{OS}, V_{RT}, -A5.2V, (2) DGND, -D2V, -D4.5 V	J151-ND	Digi-Key	Banana Plug	9
2	C2-4	PCS5106CT-ND	Digi-Key	Decoupling Capacitor	3
3	C6-11, C19,C27	PCS2106CT-ND	Digi-Key	Decoupling Capacitor	7
4	C5, C12, C50-59, C61-73, C75-77, C90-91	PCC103BCT-ND	Digi-Key	Generic SMD Capacitor Gate & Pin, Swappable	30
5	C13-18	PCS2225CT-ND	Digi-Key	Decoupling Capacitor	7
6	C20-26, C28-39 C74, C78-89	PCC104BCT-ND	Digi-Key	Generic SMD Capacitor Gate & Pin, Swappable .1 µF	32
7	C40-48	PCC101CCT-ND	Digi-Key	Generic SMD Capacitor Gate & Pin, Swappable 100 pF	9
8	CLK, DACOUT, V_{IN}	PE4117	Omni-Spectra or Pasterneck	PCB Mountable OSP Connector	3
9	D1	ICL8069ACSQ2	Maxim	-1.2 V Ref	1
10	D2-4	1N4001	Newark	Axial SS Diode with Alternate	3
11	FB1-10	P9820BK-ND	Digi-Key	Ferrite Bead	10
12	J1	137M-ND	Digi-Key	AMP 37 Pin Connector	1
13	J2-8 JA1, JB1	929838-01-36-ND	Digi-Key	Jumper Block, 2 Pins	9
14	J9	2380-6221TG-ND	Digi-Key	3 PinJumper	1
15	Q1	2N2907A-ND	DIGI-KEY	TO18 EBC PNP Small Signal Transistor	1
16	R1-4	3266W-102	Any	Potentiometer	4
17	R5	3266W-200	Any	Potentiometer	1
18	R7	3266W-102-ND	Any	Potentiometer	1
19	R6	200X-ND	Digi-Key	Socketed 1/8 W 5% Res., Ctrs:400 Res Body:60	1
20	R111	P100EMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	1
21	R26, R46	P120EMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	2
22	R10-15, R23	P1KEMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	7
23	R25	P2.7KEMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	1
24	R27-30	P22EMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	4
25	R8-9, R16-18, R22 R35, R40-45, R47-59, R62-89, R91-96, R110, R112	P49.9EMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	62
26	R24	P49R9EMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	1
27	R19-21, R31 R90	P51EMG-ND	Digi-Key	SMD 3.2 X 1.6 MM Resistor	5
28	R33-34	51X-ND	Digi-Key	Socketed 1/4 W 1% Resistor	2
29	RN3, RN5	770-61-R51-ND R7470CT-ND	Digi-Key	8-Pin SIP Resistor Pack	2
30	RN4, RN6	760-1-R51-ND 4608X-470-ND	Digi-Key	DIP Resistor 14 Pins 7 Isolated Resistors	2
31	S0-2, SW5-11	ET01MD1V3BE	Digi-Key	DPDT Switch 1:C 2:NC 3:NO	10
32	U1	SPT7610	SPT	6-Bit Flash ADC	1
33	U2	LM337H-ND	Digi-Key		1
34	U3	MC10EL16D	MOTOROLA	D Flip-Flop	1
35	U4	OP491GS	Digi-Key/ Analog Devices	Rail-to-Rail Op Amp	1
36	U5	SPT10181AIN	SPT	8-Bit Digital-to-Analog Converter	1
37	U8	MC100E167FN	Motorola/Arrow	6-Bit 2:1 Mux	1
38	U9	SY100E151J	Synergy	6-Bit D Register	1
39	U10	SY100S350JC	Synergy	Hex D-Latch	1
40	U11	MC100E196	Motorola	Prog Delay	1
41	U12	MC100EL07	Motorola	2 Input XOR/XNOR	1
42	U13	MC100EL33	Motorola	/4 Divider	1
43	U14	MC100EL34	Motorola	Clock Gen Chip	1
44	U15	MC100EL57	Motorola	4:1 Diff Multiplex	1
45	U16	MC10El11	Motorola	1:2 Fanout Buffer	1
46	AG1-2, D61-62, DG1-2, FT1, LINV1 MINV1, REF1 SB1, TEST1, TP1-3, V_{FB1}, V_{R1}, V_{R3}, V_{REF1}, V_{RM1}	40F6045	Newark	Test Point	20
47	A/R	8440GK-ND	Any	#4-40 Screw	4
48	A/R	1902EK	Any	Nylon Hex Standoff Threaded For #4-40 screw	4

Figure 10 - Component Side

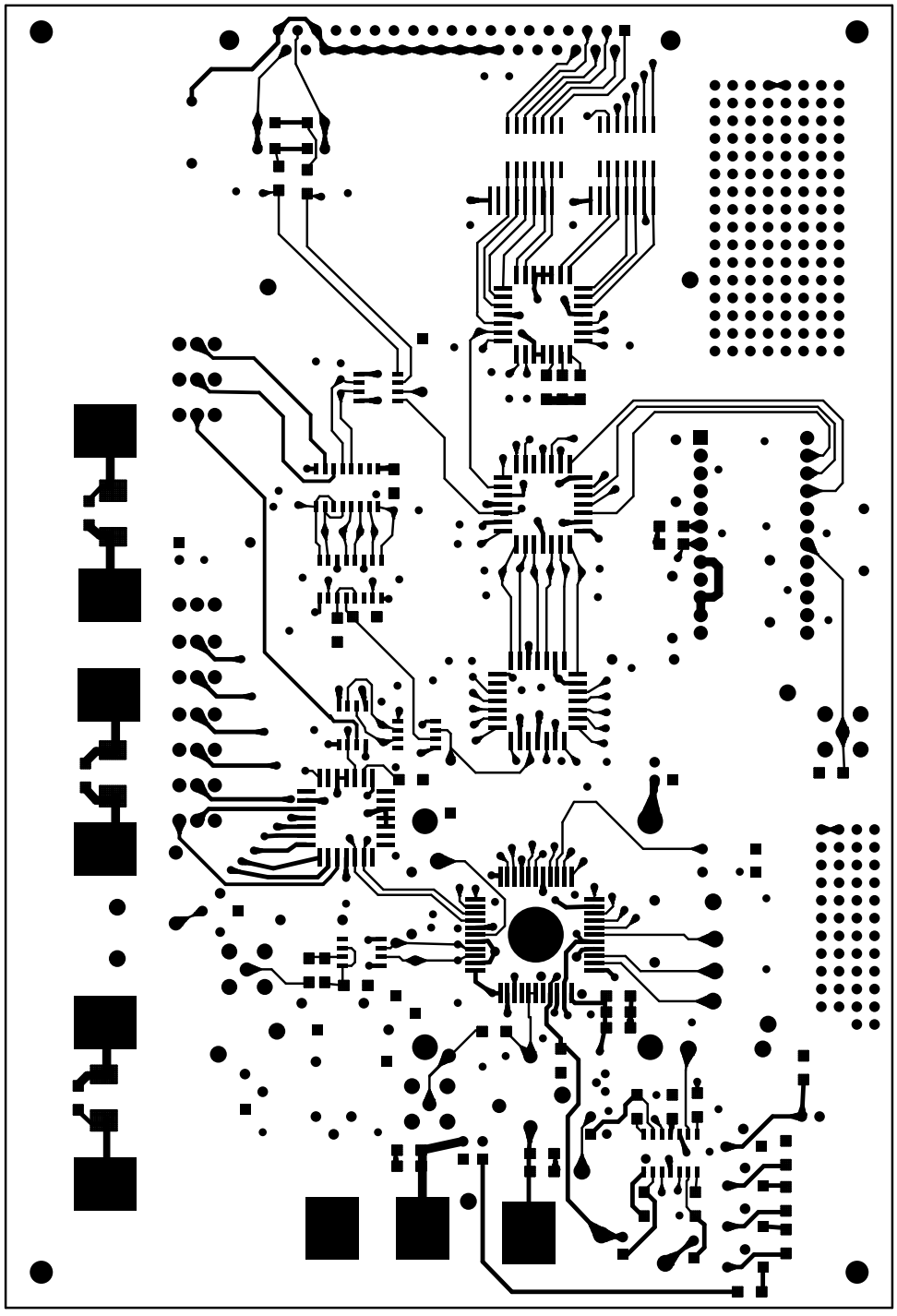


Figure 11 - Ground

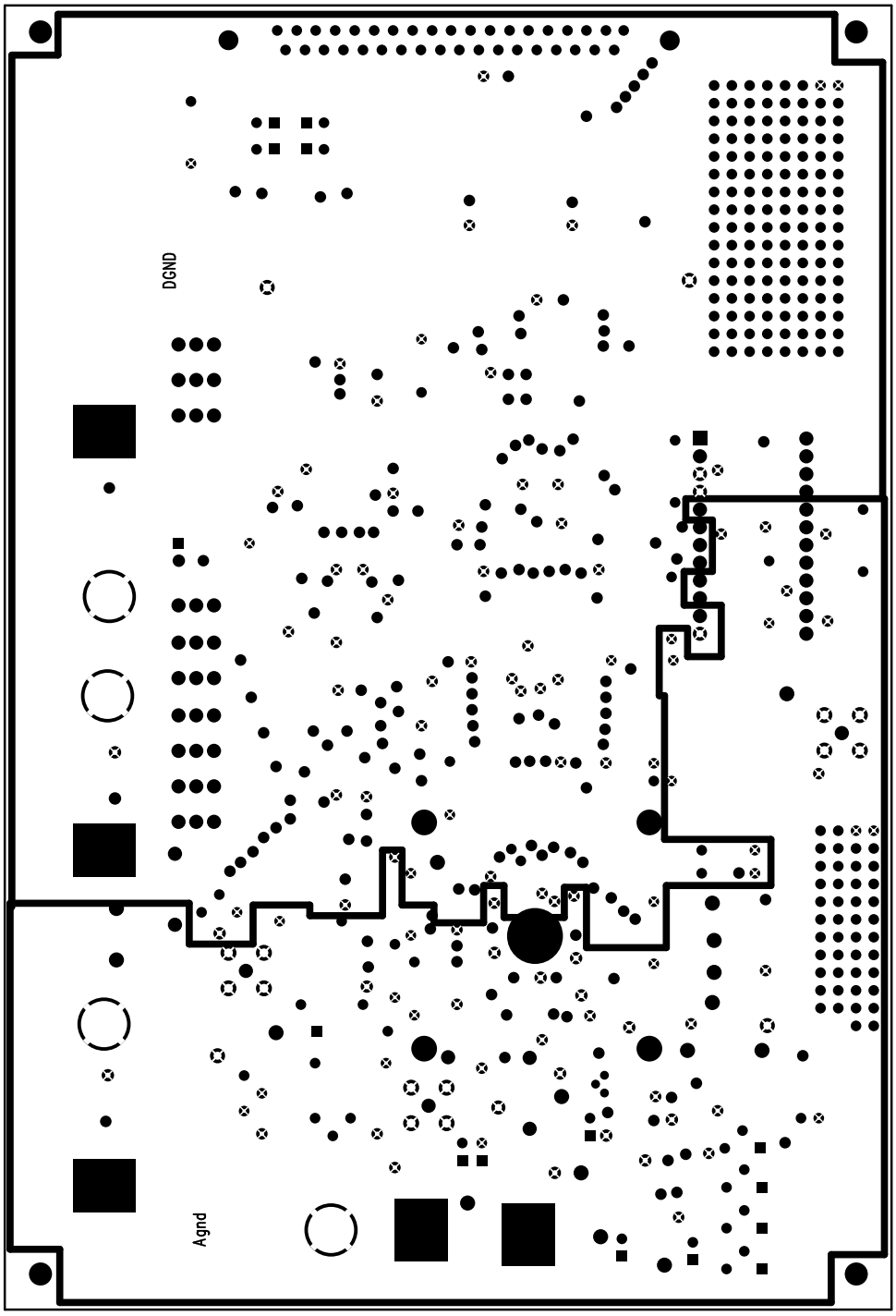


Figure 12 - Signal Layer 1

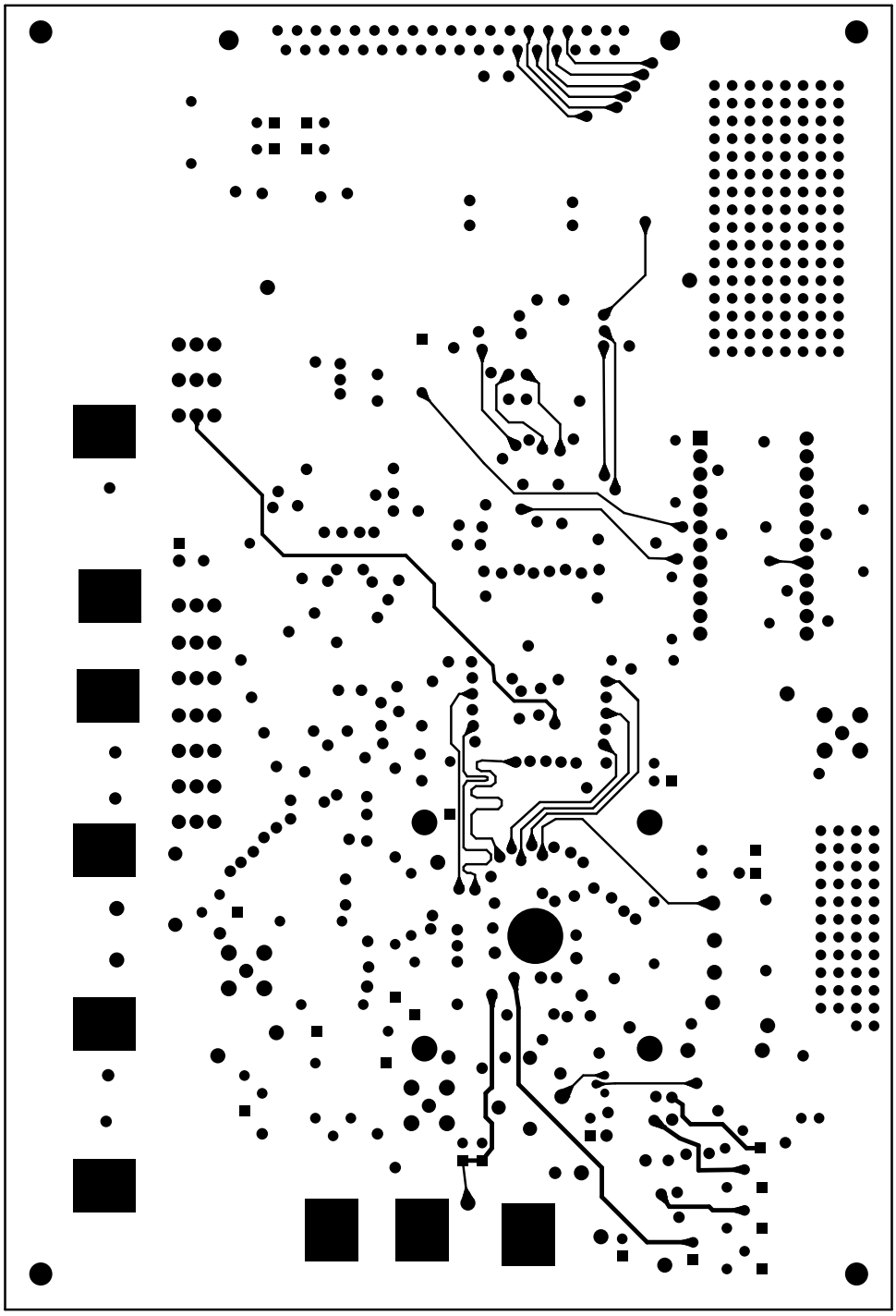


Figure 13 - Signal Layer 2

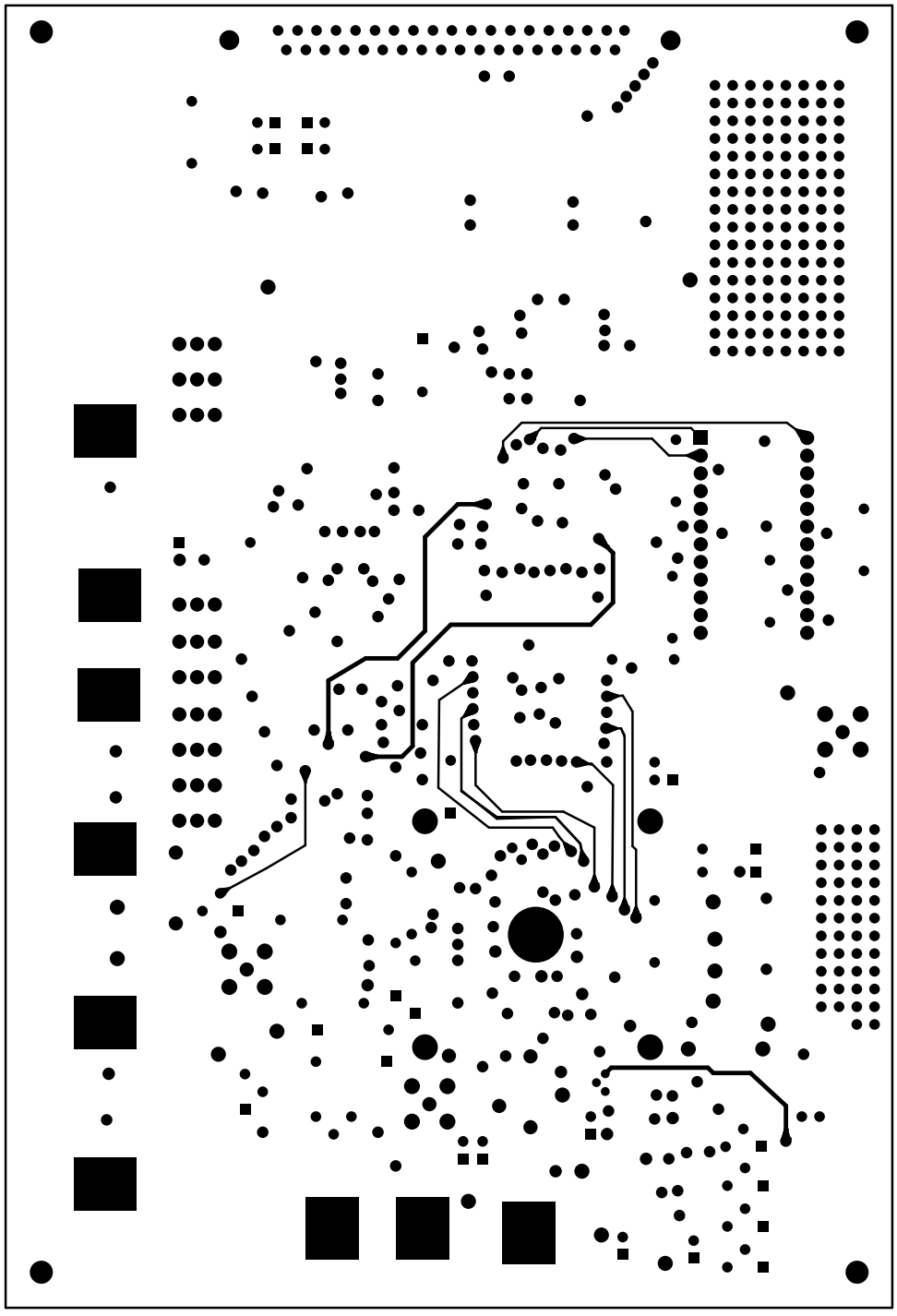


Figure 14 - Power

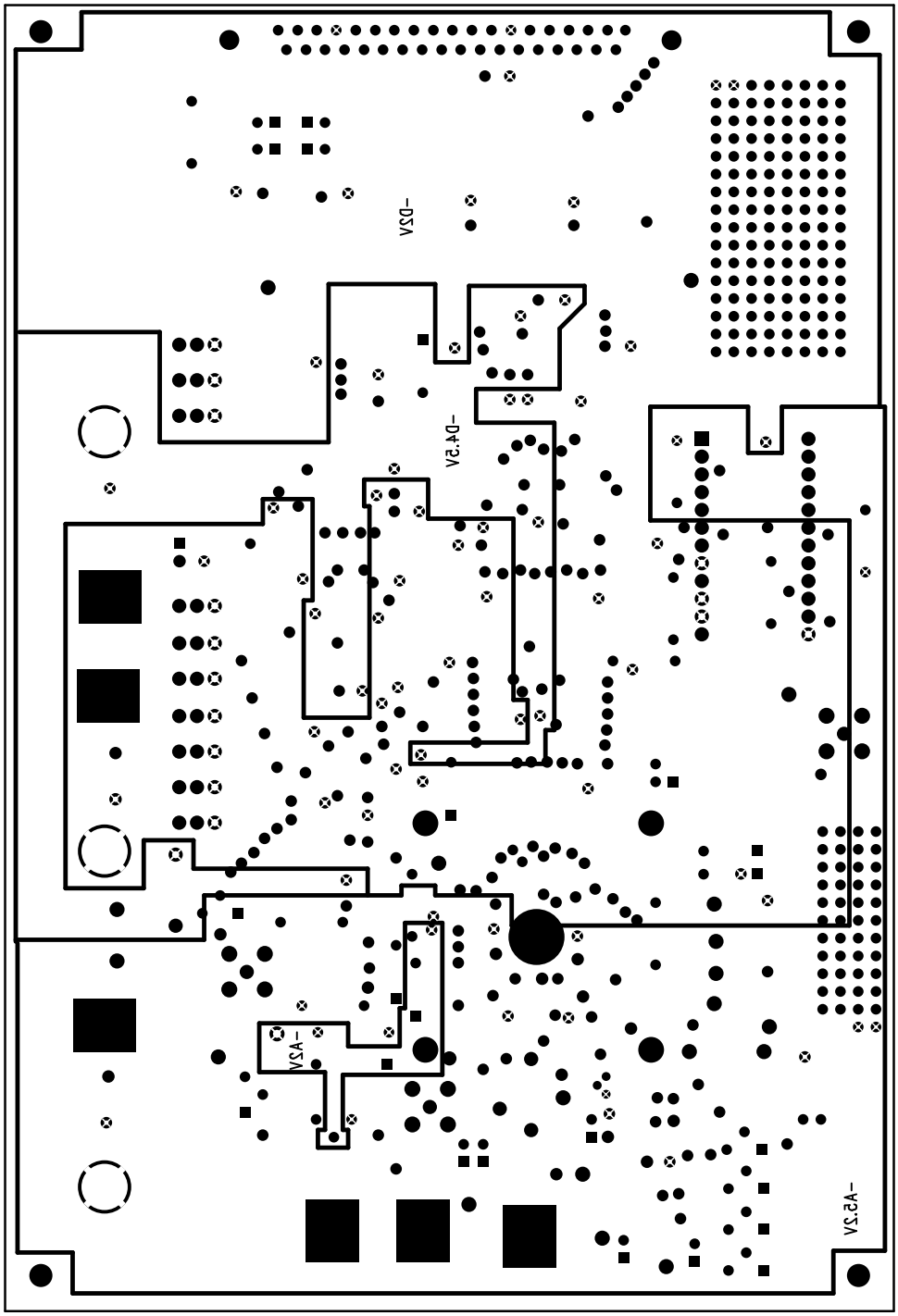


Figure 15 - Solder Side